



# YIFAN YANG

+86 1805-3228-579

[yyang593@connect.hkust-gz.edu.cn](mailto:yyang593@connect.hkust-gz.edu.cn)

[github.com/Brandonyfyang](https://github.com/Brandonyfyang)

## Research Field

- Computer Architecture
- Implementation of different algorithms based on FP-GAs

## EDUCATION

|   |   |
|---|---|
| <b>M.Phil. in Microelectronics</b>   <i>Advised by: Prof.Jiayi Huang</i><br>The Hong Kong University of Science and Technology (GuangZhou)                    | Sep. 2024 – Present   |
| <b>B.Eng. in Integrated Circuits Design and Systems</b><br>Huazhong University of Science and Technology<br>• Electronics Courses GPA: 3.92/4.0 for 62-credit | Sep. 2020 – Jun. 2024<br>CGGPA: 3.88/4.0<br>Mathematics Courses GPA: 3.97/4.0 for 24.5-credit |

## WORK EXPERIENCE

|  |                                       |
|--|---------------------------------------|
| <b>Intern (FPGA Engineer)</b>   <i>Advised by: SE ENGR Chao Xiao</i><br>Shanshui Photoelectronic Technology Co., Ltd.<br>• Implemented Ethernet Transmission Algorithms in Kindex FPGA and the bid for the project was successful. | Jul. 2023 – Dec. 2023<br>Wuhan, China |
| <b>Intern (FPGA Engineer)</b>   <i>Advised by: SE ENGR Tao Zhou</i><br>Viestar Medical Technology Co., Ltd.<br>• Implemented Image Processing Algorithms in Zynq FPGA as part of the confocal endoscope mainframe.                 | Mar. 2024 – Jul. 2024<br>Wuhan, China |

## PUBLICATIONS

[C] Y. Yang, Z. Zheng, "ECG signal classification algorithm and circuit design based on deep learning," **ICFTIC (IEEE EI)**, 2024

## RELATED PROJECTS

|  |                                       |
|--|---------------------------------------|
| <b>FPGA Embedded Chip Design Competition</b>   <i>Advised by: SE ENGR Jianxin Wu</i><br>Department of EIC,HUST<br>• Designed a bank payment system using Xilinx series FPGA, which has functions for deposit, withdrawal, and balance inquiry, including fingerprint recognition module and VGA display module.  | Aug. 2022 – Nov. 2022<br>Wuhan, China |
| <b>Development of ECG Sensing Based on FPGAs</b>   <i>Advised by: Prof. Zhaoxia Zheng</i><br>Department of ICDE,HUST<br>• Based on the Resnet model, implement CNN in the Pytorch to classify and diagnose different types of ECG signals. Besides, based on the Zynq, implement CNN and ECG classification diagnosis on it, comparing the results with the Pytorch end. | Dec. 2023 – Jun. 2024<br>Wuhan, China |

## HONORS AND AWARDS

Self Improvement Scholarship of HUST(2021) Honorable Mention of The MCM/ICM (2022)

**Excellent Award of National Undergraduate Embedded Chip Design Competition** (2022)

Scholarship for outstanding student cadres (2022)

Intel China FPGA Engineer Certificate(2023)

**Full Postgraduate Scholarship, HKUST(GZ)**(2024)

## SKILLS

**Languages:** English, Chinese Mandarin(native)  
Markdown

**Document Creation:** Microsoft Office Suite, L<sup>A</sup>T<sub>E</sub>X,

**Hardware Description Languages:** Verilog, Chisel    **Programming:** C & C++, Python

**Electronics Design Automation Software:** Xilinx Vivado, Cadence, SE Modelsim, Quartus II, Chipyard