Yifan Yang

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Education Background

Huazhong University of Science and Technology Wuhan China | 2020/09–2024/06

- **Bachelor in IC Design and Systems**
- **GPA:** 3.88/4.00 **IELTS:**6.5 (L:7.5 |R:7.5| W:6.0| S:5.5)

HKUST(GuangZhou) Guangzhou China | 2024/09–2026/10

- **MPhil in Microelectronics**
- **Research interests:** Computer Architecture, FPGA Development, Digital VLSI Design.

Relevant Courses

- **Principles of Computer Organization**, **Verilog and Digital System**, Principle and Design Fundamental of Sensors
- **Digital Signal Processing**, Signals and Linear Systems, Calculus

Internship Experience

Shanshui Optoelectronic Technology Co., Ltd.(Wuhan)-FPGA Engineer 2023/07 – 2023/12

Design of Ethernet Packet High Speed Storage and Forwarding Circuit 2023/07 – 2023/08

- Based on the DDR3 controller IP core, I designed a read-write arbitration circuit for storing and forwarding Ethernet data packets, and used PRBS15 to verify data correctness

Design of Ethernet message sending/receiving parsing Circuit 2023/09 – 2023/10

- Sender: Extract IP packets in vlan frame format from the physical layer, determine whether to delete vlan frames, add FCS frames, and perform FCS verification; Store and forward processed packets and input them into DDR3
- Receiver: Receive vlan packets stored in DDR3, implement storage and forwarding, and determine whether to add vlan frames and delete FCS frames

Communication Circuit Design Based on PCM30 2023/11 – 2023/12

- Based on Gowin series chips, achieve multiplexing and demultiplexing of 8 channels for PCM complex frames
- Supports PCM framing, decoding, alarm processing, and supports rate adjustment and clock management for PCM communication services

Viestar Medical Technology (Wuhan) Co., LTD-FPGA Engineer 2024/03 – 2024/06

Design of distortion correction algorithm module 2024/03 – 2024/04

- The image obtained by sine wave sampling with equal time interval is mapped to the image obtained by sampling with equal distance interval.The center column of the sample and the scaling factor are configurable.
- Open root and inverse cosine functions are realized indirectly by CORDIC IP core.

Design of sampling control algorithm module 2024/04 – 2024/05

- The sampling delay control logic is designed so that the data sampling interval can cover all levels of the synchronous signal.
- The sampling mode can be configured into single/double edge sampling and single/double speed sampling.

Image processing algorithm: line alignment algorithm design 2024/06 – 2024/06

- Based on Zynq series FPGA, 21 consecutive frames of data collected by confocal probe are aligned in line, and each frame is stored by DDR3.
- The DMA transmission module of image after line alignment processing is designed to realize data transmission at PL and PS terminals.

Research and Competition Experience

FPGA Embedded Chip Design Competition 2022/08 – 2022/11

Supervisor:Senior Engineer Wu Jianxin

- Designed a bank payment system using Xilinx series FPGA, which has functions for deposit, withdrawal, and balance inquiry, including fingerprint recognition module and VGA display module.
- Completed circuit design, simulation, functional verification, and implementation using Verilog language on Vivado.

Development of ECG Sensing Chip(Graduation project) 2023/12 – 2024/06

Supervisor:Professor Zheng Zhaoxia

- Based on the Resnet network model, implement CNN in the Pytorch framework to classify and diagnose different types of electrocardiogram signals.
- Based on the Zynq series FPGA, implement CNN and ECG classification diagnosis on chip, and compare the results with the software end.
- Optimized on-chip matrix convolution and CNN computation process based on Systolic Array.

Patents

- Zhaoxia Zheng, **Yifan Yang**, Zengbao Xing, Gang Zheng,"Implementation of an ECG classification method based on CNN"(in application)

Honors and Awards

- Self Improvement Scholarship of HUST(2021)
- Honorable Mention of The Mathematics Contest in Modeling of America (2022)
- **Excellent Award of National Undergraduate Embedded Chip Design Competition** (2022)
- Scholarship for outstanding student cadres (2022)
- **Full Postgraduate Scholarship, HKUST(GZ)**(2023)
- Intel China FPGA Engineer Certificate(2023)

Skills and Interests

- **Programming Languages:** Verilog HDL, C, Python.
- **Development tools/platforms:** Vivado, Quartus II, SE Modelsim, LaTeX.